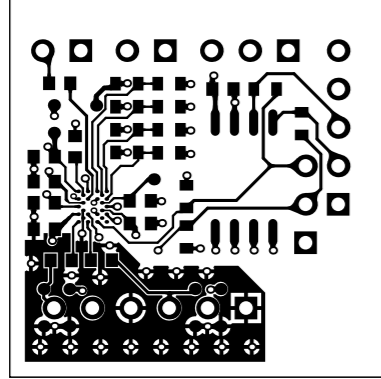
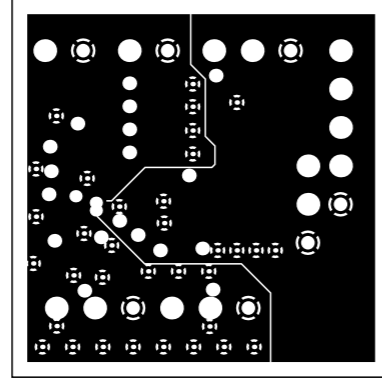


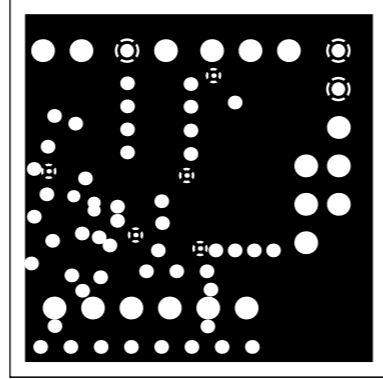
Copper top (scale 2)



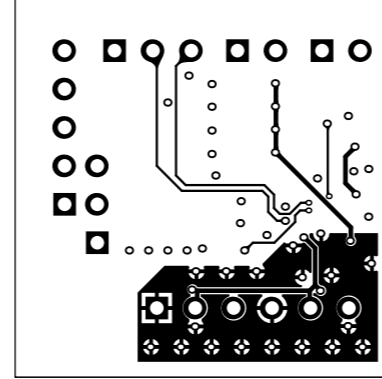
Inner layer 1 - Ground (scale 2)



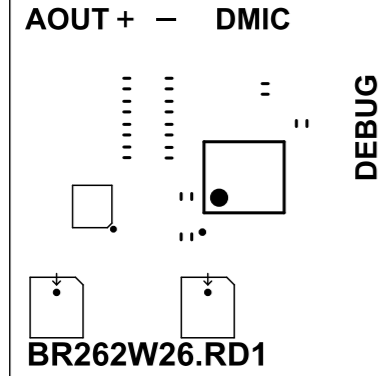
Inner layer 2 - VBAT (scale 2)



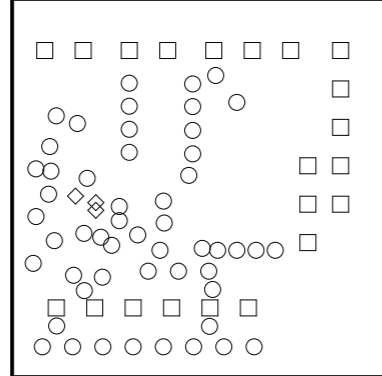
Copper bottom view (scale 2)



Silkscreen top (scale 2)



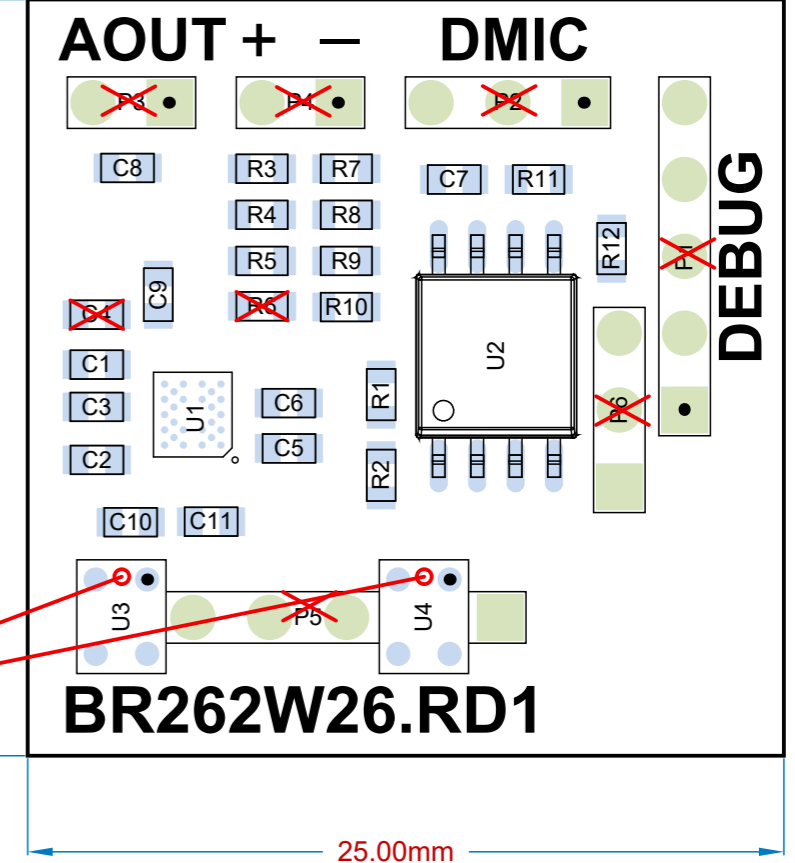
Drill Drawing View (scale 2)



Drill Table

Symbol	Count	Hole Size	Plated	Via / Pad
◇	3	0.20mm(8mil)	Plated	Via
○	52	0.30mm(12mil)	Plated	Via
□	21	0.90mm(35mil)	Plated	Pad
	76 Total			

Assembly view top (scale 4)

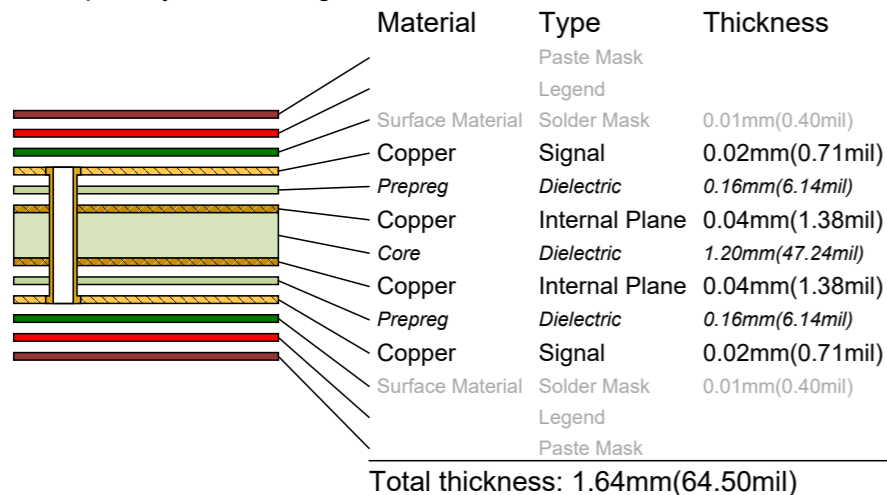


Acoustic port position

Notes:

- Board material FR4 RoHS Compliant with nominal thickness, 35 um copper on all layers
- Order of layers is top, inner1, inner2, bottom
- Green L.P.1 mask both sides. Mask must be between all lands. Minimum of 38um per side around WLCSP (U1)
- Silkscreen to be white ink on component side of board. No ink to be on surface mount land pads.
- Boards to be 100% tested to Gerber net list file
- Do not insert: C4, R6 and P1-P6
- Surface mount components: Top side 23
- Include a minimum of two fiducials per panel
- V-score routing
- VBAT on P4: 1.65Vdc to 3.6 Vdc
- QR Code to: www.sallberg.at/br262rd1
- Test points:
 1. Ground
 2. VREG: 0.95V to 1.05V, nominal 1.0V
 3. VDDA: 1.8V to 2.1V, nominal 2.0V
 4. VDDD: 1.62V to 1.98V, nominal 1.7V

Example Layer Stack Legend



Bill Of Materials

Item	Designator	Type	Part	Quantity
1	C1-C3, C5, C6	CAP CER 1UF 6.3V X5R 0603	CAP CER 1UF 6.3V X5R 0603	5
2	C10, C11	CAP CER 10NF 10V X7R 0603	CAP CER 10NF 10V X7R 0603	2
3	C4	CAP CER 0000	CAP CER 0603	1
4	C8	CAP CER 2.2UF 10V X5R 0603	CAP CER 2.2UF 10V X5R 0603	1
5	C7, C9	CAP CER 100NF 6.3V X7R 0603	CAP CER 100NF 6.3V X7R 0603	2
6	R1, R2, R10	RES SMD 10K OHM 1% 0.1W 0603	RES SMD 10K OHM 1% 0.1W 0603	3
7	R11, R12	RES SMD 47 OHM 1% 0.1W 0603	RES SMD 10K OHM 1% 0.1W 0603	2
8	R4, R9	RES SMD 75K OHM 1% 0.1W 0603	RES SMD 75K OHM 1% 0.1W 0603	2
9	R6	RES SMD DNI 0603	RES SMD DNI 0603	1
10	R7	RES SMD 39K OHM 1% 0.1W 0603	RES SMD 39K OHM 1% 0.1W 0603	1
11	R3, R5, R8	RES SMD 100K OHM 1% 0.1W 0603	RES SMD 100K OHM 1% 0.1W 0603	3
12	U1	BR262W26A103E1G	BR262W26A103E1G, Wideband Noise Reduction	1
13	U2	CAT24C64WI-GT3	IC EEPROM 64KBIT 400KHZ 8SOIC	1
14	U3, U4	SPU0410HR5H-PB	MIC MEMS ANALOG OMNI -42DB	2

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: +/- 100um		FINISH: Soft Gold		DEBURR AND BREAK SHARP EDGES		DO NOT SCALE DRAWING		REVISION	
DRAW Sällberg		SIGNATURE		DATA		TITLE:		BR262 Reference Design 1	
CHK'D		MFG		QA		MATERIAL:		DWG NO.	
						FR4 - 4 layers, standard thickness		A0	
						WEIGHT:		SCALE 1:1	
								SHEET 1 OF 1	