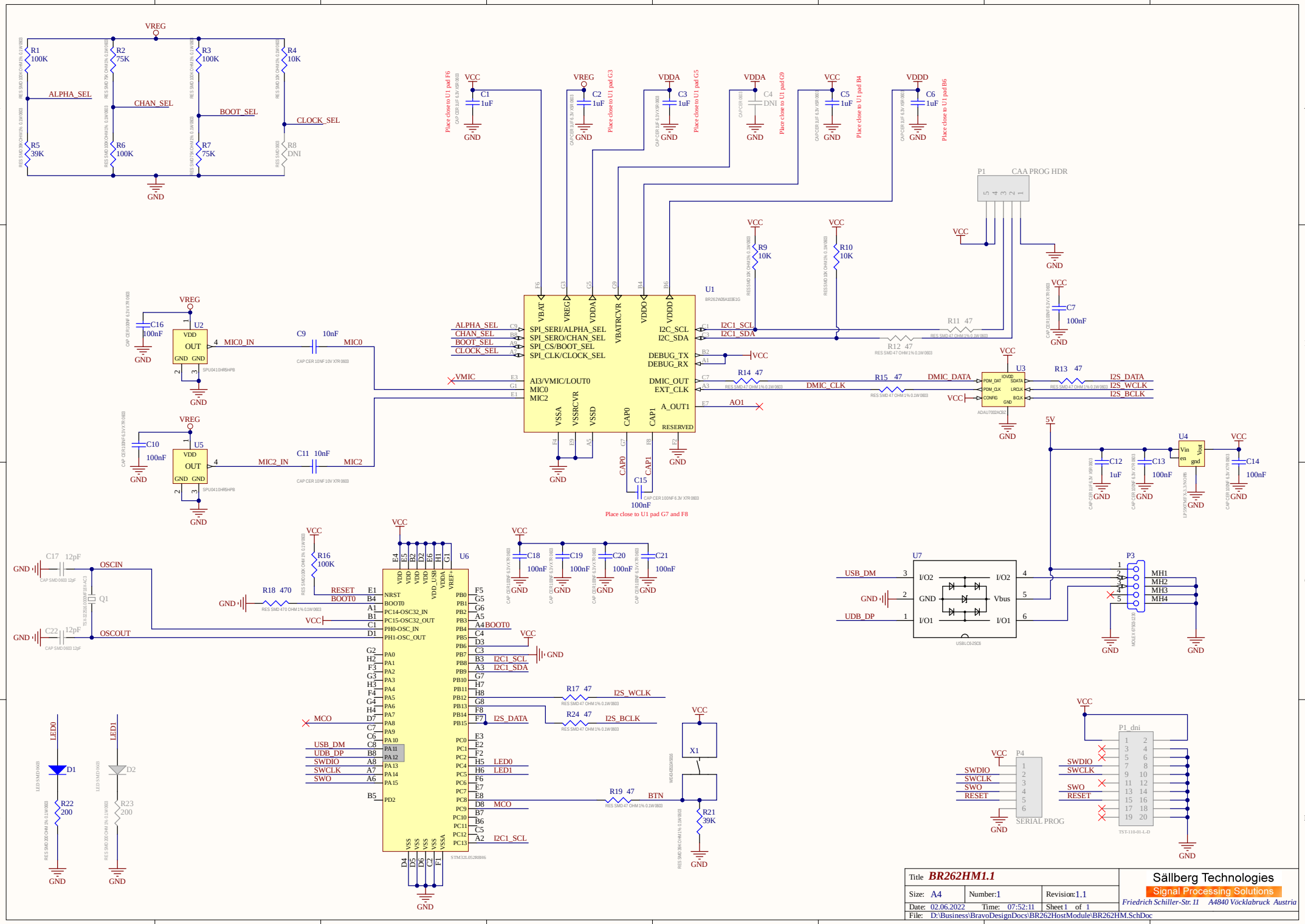
VREG
R1 100K
R2 75K
R3 100K
R4 10K
ALPHA_SEL
CHAN_SEL
BOOT_SEL
CLOCK_SEL
R5 39K
R6 100K
R7 75K
R8 DNI
GND
VCC
C1 1uF
C2 1uF
C3 1uF
C4 DNI
C5 1uF
C6 1uF
VDDA
VDDD
Place close to U1 pad F6
Place close to U1 pad G3
Place close to U1 pad G5
Place close to U1 pad G9
Place close to U1 pad B4
Place close to U1 pad B6
P1 CAA PROG HDR
R9 10K
R10 10K
U1
BR262W06A303E1G
VBAT
VREG
VDDA
VBATRCVR
VDDO
VDDD
SPI_SERI/ALPHA_SEL
SPI_SERO/CHAN_SEL
SPI_CS/BOOT_SEL
SPI_CLK/CLOCK_SEL
I2C_SCL
I2C_SDA
DEBUG_TX
DEBUG_RX
AI3/VMIC/LOUT0
MIC0
MIC2
DMIC_OUT
EXT_CLK
A_OUT1
RESERVED
VSSA
VSSRCVR
VSSD
CAP0
CAP1
I2C1_SCL
I2C1_SDA
R11 47
R12 47
C7 100nF
C16 100nF
U2
VDD
OUT
GND
MIC0_IN
C9 10nF
MIC0
VMIC
C10 100nF
U5
MIC2_IN
C11 10nF
MIC2
C15 100nF
Place close to U1 pad G7 and F8
R14 47
R15 47
DMIC_DATA
DMIC_CLK
U3
ADAU7002ACBZ
R13 47
I2S_DATA
I2S_WCLK
I2S_BCLK
AO1
5V
U4
Vin
Vout
en
gnd
C12 1uF
C13 100nF
C14 100nF
C17 12pF
C22 12pF
OSCIN
OSCOUT
Q1
R16 100K
R18 470
RESET
BOOT0
U6
STM32L052R8H6
PC14-OSC32_IN
PC15-OSC32_OUT
PH0-OSC_IN
PH1-OSC_OUT
VDD_USB
VREF+
C18 100nF
C19 100nF
C20 100nF
C21 100nF
USB_DM
UDB_DP
SWDIO
SWCLK
SWO
MCO
LED0
LED1
R17 47
R24 47
R19 47
BTN
X1
R21 39K
D1
D2
R22 200
R23 200
U7
USBLC6-2SC6
I/O2
GND
I/O1
Vbus
P3
MH1
MH2
MH3
MH4
P4
SERIAL PROG
P1_dni
TST-110-01-L-D
Title BR262HM1.1
Size: A4
Number: 1
Revision: 1.1
Date: 02.06.2022
Time: 07:52:11
Sheet 1 of 1
File: D:\Business\BravoDesignDocs\BR262HostModule\BR262HM.SchDoc
Sällberg Technologies
Signal Processing Solutions
Friedrich Schiller-Str. 11 A4840 Vöcklabruck Austria